REMARKS

Claims 1-22 are currently pending in the application. Claims 1-22 were rejected. Claims 1 and 21 have been amended. Claims 9 and 22 have been canceled without prejudice.

The Examiner rejected claims 1-22 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The Examiner stated that the present application does not specify which signals are the first, second, and third calibration signals recited in the claims. In addition, the Examiner stated that the terms "calibration mode" and "normal operation mode" are not sufficiently descriptive to allow one of ordinary skill in the art to make or use the invention. The rejection is respectfully traversed.

The Summary of the Invention clearly refers to the calibration and normal operation modes recited in the claims of the present application. And beginning at paragraph [0022], the present application describes a specific embodiment of the invention with reference to Figs. 1-3, clearly referring to both modes. For example, in paragraph [0023], the present application states that " [w]hen amplification is called for ..., actual amplification is temporarily held off, " and that "[a]fter a stabilization delay..., DC offset cancellation logic 106 takes over control of the Y and YB outputs of processor 106 (and therefore the V+ and V- amplifier outputs) for the duration of the DC offset cancellation sequence." When coupled with the subsequent description in paragraphs [0024]-[0026] and the timing diagram of Fig. 3, it is clear to even the casual reader that a calibration mode has been entered during which offset cancellation signals are generated. Further, in paragraph [0026], the present application states that "[w]hen counter B reaches zero, both counters A and B are stopped..., and DC *calibration* for the channel is complete. The Y and YB outputs of the processor once again are set to respond to the COMP signal, closing the *normal* loop... *Normal* switching amplification begins." Emphasis added.

And, it would be a trivial exercise for one of ordinary skill in the art to design something which is operable to take "over control of the Y and YB outputs of processor 106," and then to

subsequently set the "Y and YB outputs of the processor once again...to respond to the COMP signal."

Similarly, it would be clear to one of ordinary skill in the art which signals in the detailed description of the present application can be mapped to the offset cancellation signals recited in the claims. For example, in the exemplary embodiment illustrated in the timing diagram of Fig. 3, voltage signals V1, V2, and V3 map to the first, second, and third offset cancellation signals recited in claim 1, respectively. With such a straightforward and obvious mapping, nothing further is required.

In view of the foregoing, the rejection of the claims under section 112, first paragraph, should be withdrawn.

The Examiner rejected claims 1-8 and 10-22 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,724,248 (the '248 patent). The Examiner indicated that the subject matter of claim 9 corresponded to patentable subject matter. Claims 1 and 21 have been amended to incorporate limitations similar to those recited in claim 9. The rejection of claims 1-8 and 10-21 is believed overcome thereby.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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